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10/684,706	10/14/2003	Kimble Dong	004320.P006C	4838
62294 7590 08/19/2008 BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP 1279 Oakmead Parkway			EXAMINER	
			AGGARWAL, YOGESH K	
Sunnyvale, CA 94085-4040			ART UNIT	PAPER NUMBER
			2622	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)			
	10/684,706	DONG, KIMBLE			
Office Action Summary	Examiner	Art Unit			
	YOGESH K. AGGARWAL	2622			
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).			
Status					
Responsive to communication(s) filed on <u>06 Mar</u> This action is FINAL . 2b) ☑ This Since this application is in condition for alloward closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro				
Disposition of Claims					
4) Claim(s) 1,3-7,21,22 and 24-27 is/are pending 4a) Of the above claim(s) is/are withdrav 5) Claim(s) 1 and 3-7 is/are allowed. 6) Claim(s) 21,22 and 24-27 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or	vn from consideration.				
9)☐ The specification is objected to by the Examine	r				
10) The drawing(s) filed on is/are: a) access applicant may not request that any objection to the confidence of th	epted or b) objected to by the Edrawing(s) be held in abeyance. See on is required if the drawing(s) is obj	e 37 CFR 1.85(a). lected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	nte			

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Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 21, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rambaldi (US Patent # 6,618,084) in view of Houchin et al. (US Patent # 5,047,861). [Claim 21]

With regard to claim 1 Rambaldi et al. disclose a MOS image sensor comprising: a pixel array formed from a plurality of pixels arranged in a matrix of rows and columns (pixel array area sensor 12, FIG. 1); location processing means for providing a digital location number for each pixel of the pixel array (column 9 lines 33-45) [while no specific location processing means are disclosed it is inherent that one must exist in order for the disclosed storing of the location to be accomplished, if no location processing means existed it would be impossible to determine what location to store for the defective pixels]; signal processing circuitry for reading out signals from the pixel array and outputting processed pixel signals (analog to digital converter 18, FIG. 1); dead pixel comparator circuitry for receiving the processed pixel signals from the signal processing circuitry and examining the processed pixel signals to see if they are indicative of dead pixels (fault analysis and correction block 24, FIG. 1, column 9 lines 19-33); location storage circuitry for receiving dead pixel information from the dead pixel comparator circuitry and for storing the digital location number generated by the location processing means for each dead pixel, wherein digital location numbers are stored in the location storage circuitry only for

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pixels that are determines to be dead pixels (memory 26, FIG. 1, column 9 lines 33-45); and location comparator circuitry for comparing the digital location number of a pixel that is being processed by the signal processing circuitry with the stored digital location numbers of dead pixels to determine if the pixel that is being processed corresponds to a dead pixel (fault correction block 24, FIG. 1, column 9 line 56 - column 10 line 45), wherein the pixel array and the dead pixel comparator circuitry are formed on a single integrated circuit (column 5 lines 29-35).

Rambaldi et al. disclose the image sensor of claim 1, but fail to disclose wherein the location processing means comprises a location shift register for indicating the digital location number of each of the pixels to the pixel array, the location comparator circuitry and the location storage circuitry. Houchin discloses The addressing of memory 40 is controlled by the output from address counter 50 which also controls the clock circuits 12 which control the readout sequence of image sensor 10 (col. 3 lines 45-48). It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor of Rambaldi et al. to include the pixel address counter of Houchin in order to know the exact pixel address currently being scanned.

- 3. With regard to claim 22 Rambaldi et al. disclose wherein the pixel array, the signal processing circuitry, and the dead pixel c0mparator circuitry are fabricated on a single MOS chip. It would have been obvious to include the location shift register of Houchin as part of that single chip in order to continue the process of creating compact circuitry for the camera device.
- 4. All limitations of claim 24 are addressed in the rejection of claim 21, claim 24 is likewise rejected.

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5. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rambaldi et al. (US Patent 6,618,084) in view of Houchin et al. (US Patent # 5,047,861) and Liang et al. (US Patent 5,781,233).

- 20. Claim 25 is rejected under the same analysis as claim 21, further Rambaldi et al. and Houchin et al. fail to disclose a means for precharging the plurality of pixels to a fixed voltage. Liang et al. disclose a means for precharging the plurality of pixels to a fixed voltage (column 6 lines 38-52). It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor of Rambaldi et al. and Houchin et al. to include the precharging function taught by Liang et al. in order to provide signal amplification of the pixel signal (column 3 lines 9-13).
- 6. Claim 26 is rejected under the same analysis as claim 22. All limitations of claim 27 are addressed in the rejection of claim 21, claim 27 is likewise rejected.

Allowable Subject Matter

7. Claims 1, 3-7 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOGESH K. AGGARWAL whose telephone number is (571)272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yogesh K Aggarwal/ Primary Examiner, Art Unit 2622